wherein:

the global wiring layer comprises:

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer; and

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring within the system LSI cell portion, and electrical interconnection between gates of different said the functional blocks is provided by the global wiring layer.--

Amend claim 6 as follows:

--6. (twice amended) A system semiconductor device, comprising:

a system LSI cell portion comprising a semiconductor chip divided into a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip, each of the functional blocks comprising a plurality of gates; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

wherein the global wiring layer comprises:

a first wiring layer formed on an organic substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer, and

inner bumps formed on the second wiring layer; and

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring within the system LSI cell portion, and electrical interconnection between gates of different said the functional blocks is provided by the global wiring layer.--

Amend claim 12 as follows:

--12. (twice amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which are constructed to serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer separate from the fabricated system LSI cell portion by forming a wiring layer on a

semiconductor substrate, and

laminating the system LSI cell portion with the separately fabricated global wiring layer such that electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer.--

Amend claim 16 as follows:

--16. (twice amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, a second wiring

layer, an insulating layer, and inner bumps on the semiconductor substrate.--

Amend claim 17 as follows:

--17. (amended) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates, the semiconductor chip being formed so that electrical interconnection among said gates within a respective one of the functional blocks is provided by wiring within the LSI cell portion,

fabricating a global wiring layer by forming a wiring layer on a semiconductor substrate, and

laminating the system LSI cell portion with the global wiring layer such that electrical interconnection among said gates disposed in separate said functional blocks are electrically connected to each other by the global wiring layer;

wherein the global wiring layer is formed by sequentially laminating a first wiring layer, an insulating layer, a second wiring layer, and inner bumps on an organic substrate.--

Add the following new claim:

--24. (new) A system semiconductor device, comprising:

a system LSI cell portion comprising a semiconductor chip divided into a plurality of functional blocks which serve as unit circuits and realize specific functions on a semiconductor chip, each of the functional blocks comprising a plurality of gates; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

wherein said gates within a respective one of the functional blocks are electrically interconnected by wiring within the system LSI cell portion, and electrical interconnection between gates of different said functional blocks is provided by the global wiring layer.--

Please charge the fee of $84 for the extra independent claim added herewith, to Deposit Account No. 25-0120.

REMARKS

This application has been amended so as to place it in condition for allowance at the time of the next Official Action.

The Official Action rejects claims 1, 2, 6, 7, and 9-23 under 35 USC §102(b) as being anticipated by SAITOU et al. 5,162,240. Reconsideration and withdrawal of this rejection are respectfully requested for the following reasons:

As noted throughout the present application, including the paragraph beginning on page 3, line 13, the invention